



YESvGaN



Wide bandgap power at silicon cost

Newsletter 1 – April 2022

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Introduction

Efficient power conversion is key for the transformation towards a sustainable, electrified future in Europe. To that end, 23 European partners from research to industry united their semiconductor and power electronics expertise under the ECSEL-funded project YESvGaN. The ambitious YESvGaN goal is to establish a new class of power transistors based on Gallium Nitride (GaN) which combines the efficiency of wide band gap semiconductors with the cost benefits of silicon technology. This will be enabled by innovative vertical transistor architectures on heteroepitaxial GaN layers on low-cost substrates.

However, in order to fully demonstrate the advantages of these new power transistors, new developments are required along the whole value chain from epitaxial growth, over process and interconnection technology up the converter application level. This newsletter summarizes the key activities and achievements of YESvGaN during the first project year.

Development of vertical drift epitaxy

Epitaxy development covers a wide range of the supply chain, ranging from MOCVD equipment, over actual epitaxial growth to test devices including characterization technique during growth, after growth and after device manufacturing.

Vertical drift layer stacks have been grown on Si and Sapphire with a diode breakdown close to 400 V already at this early stage of the project. Novel characterization methods such as X-ray topography have been employed and important parameters such as defect density, drift layer conductivity and mobility as well as wafer and lattice bow have been extracted. 300 mm equipment has been designed and planned within this project and a demo system is currently under assembly. Using novel growth methods has allowed to grow crack-free 4 μm layers on top of a patterned GaN-on-Si template that will open the space to 1200 V and beyond.

Vertical breakdown

Threading dislocation Map 21x21 μm

Green = Edge-type
Blue = Screw-type

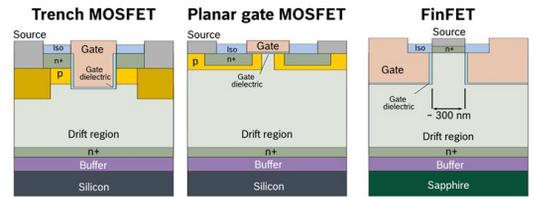
Highlights of WP2

300 mm reactor

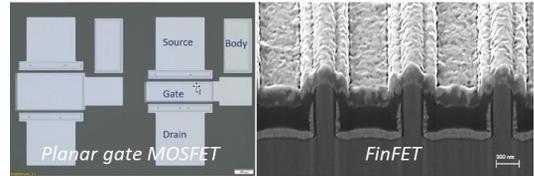
Beyond 1200 V epitaxy
4.15 μm GaN

Development of vertical GaN power transistors

Frontside chip development is focused on the design, simulation, fabrication and characterization of vertical GaN power transistors. YESvGaN targets three different transistor architectures on either silicon or sapphire substrates: Trench-gate MOSFETs, Planar-gate MOSFETs, and FinFETs. In this first year of the project, several short-loops and first device demonstrators such as Schottky diodes have already been realized. Specific focus is also given on the ion implantation process for which a dedicated ion implanter demonstrator is being developed. Several advanced characterization techniques such as XPS, Raman thermography, electrical and optical spectroscopy, are used to investigate semiconductor/gate dielectric interface and to model failure mechanics as well as their dependence on device structure/doping level.

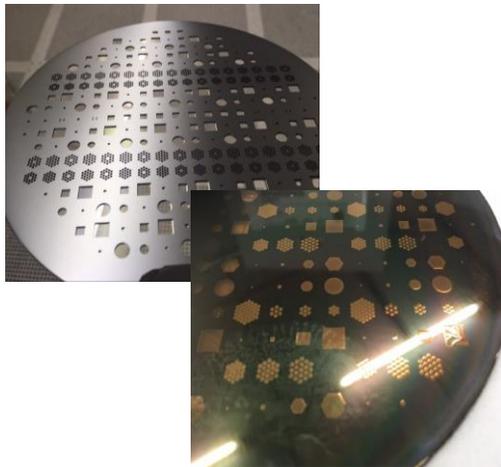


Vertical transistors structure



Device fabrication

Backside access and membrane processing

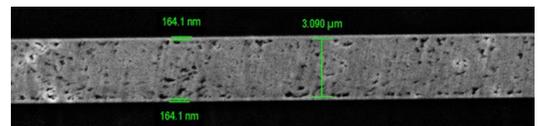
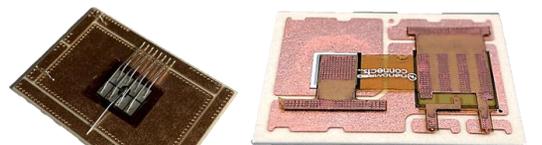


The membrane power device technology requires a set of processes, which are new in power device technology and unique in their combination, even though several process steps have been applied in other areas of semiconductor technology. The major process steps to be developed are membrane handling, i.e. temporary bonding onto a carrier wafers and debonding of the carrier, backside trenching for the Si route, i.e. local substrate and buffer removal, contact metal deposition and thermal contact formation and finally backside thick drain metallization. For the sapphire route a laser-lift-process for complete substrate removal and metal bonding are under development. Local substrate removal, membrane handling and ohmic contact formation has been successfully demonstrated on wafer level.

Assembly and reliability characterization

Assembly technology essentially determines the performance of power electronic systems. Reliable heat dissipation must always be ensured so that the maximum operating temperature of the components are not exceeded.

Because wide band gap semiconductors have a high operating temperature, the assembly technology must offer operating temperatures of more than 250°C. Within YESvGaN it is planned to adapt well-known and established technologies like soldering and sintering as well as the development of completely new technologies like nanowire-based interconnections or direct sintering techniques. All technologies are to be tested and characterized by modern scientific methods and established automotive testing norms, like AQG324.

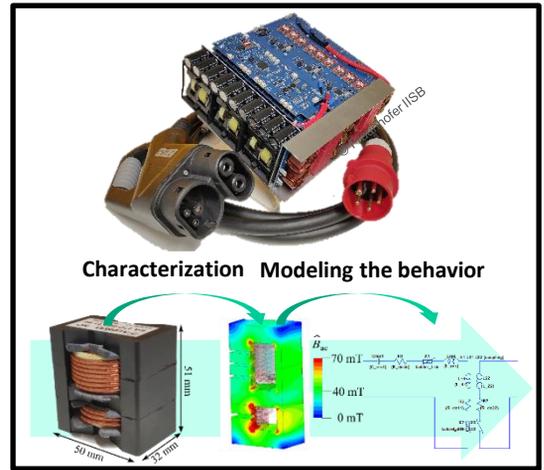


Application efficiency

The achievable improvements by the new vertical GaN transistors in power electronic systems are going to be demonstrated by means of system simulation and different application-oriented demonstrators.

In the first project year, the electrical requirements for the vertical GaN power transistors were specified from the point of view of the different target applications.

Furthermore, the selected target applications served as a starting point for the development of virtual prototypes, which enable early statements to be made about the performance of the transistors to be developed. The involved project partners transferred their prototype system into circuit simulations by characterizing the components and modeling their behavior in a digital twin. The built virtual prototypes were finally compared with measurements from the systems built in the lab and demonstrated good agreement.



Closing words

Thanks to the dedication of the YESvGaN partners, there have been impressive developments already in the first year of the project. However, there is little doubt that there are still numerous challenges ahead. Now, YESvGaN has to increasingly focus on combining the individual building blocks from this year into fully functional demonstrators which can be interconnected and evaluated in actual circuits. Thus, we are confident that the second project year will be extremely interesting and mark a significant step forward on the route towards full vertical GaN membrane transistors.

So, can we contribute to a sustainable electrified future with energy-efficient low-cost vertical GaN technology? Our answer remains clear: YESvGaN!

Future events

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|-----------------|--|
| May 9-12 | Our partners are presenting at CSMANTECH 2022 in Monterey, US |
| June 20-22 | Meet our partners at the GaN marathon 2022 in Venice, Italy |
| July 11-15 | Lectures of our partners at the SSIE summer school in Brixen, Italy |
| September 26-29 | View the work of our partners at ESREF 2022 in Berlin, Germany |
| October 09-14 | Listen to an invited talk about YESvGaN at IWN 2022 in Berlin, Germany |

Popular press



@EVGroup is the first semiconductor equipment supplier ever that receives a preferred supplier certificate from #Bosch. Proud to co-operate with both in the #YESvGaN project. Read the news [here](#).



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